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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
LEE, HSIEN MING

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 12/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/085,903

Applicant(s)

WEI ET AL.

Examiner

Hsien-Ming Lee

Art Unit

2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 10/9/03.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-4, 6-17 and 20-33 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-4, 6-17 and 20-33 is/are rejected.
- 7) ☒ Claim(s) 7 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Remarks

1. Applicant's cancellation to claims 5, 18 and 19 is acknowledged. Claims 1-4, 6-17 and 20-33 are pending in the application.

Claim Objections

2. Amended claim 7 is objected to because of the following informalities: lacking antecedent basis, i.e. "the semiconductor-on-insulator substrate." Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-4, 6-17 and 20-33 are rejected under 35 U.S.C. 102(b) as being anticipated by Yoshimi et al. (US 5,698,869).

In re claims 1 and 4, Yoshimi et al., in Fig. 7 and related text, expressly teach the claimed method of processing, comprising:

- forming an impurity region 206 (n⁺ region) in a device region 203/206/207 of a semiconductor-on-insulator substrate 201/202/Si layer, the impurity region 206 defining a pn junction 215;
- forming a buried amorphous region in the device region 203/206/207, i.e. forming a buried amorphous silicon layer, wherein the 203/206 resides, on a

buried amorphous insulating layer 202 as the semiconductor-on-insulator substrate (col. 2, lines 15-27; col. 35, lines 6-16);

- forming a dislocation region D in the device region 203/206/207 by annealing the semiconductor-on-insulating substrate to recrystallize the buried amorphous region (col. 34, line 58 through col. 35, line 16), the dislocation region D traversing the pn junctions 215 (col. 4, lines 30-33); and
- forming a gate electrode 205 on the device region 203/206/207.

In re claims 7 and 11, Yoshimi et al., in Fig. 7 and related text, also teach the claimed method of processing, comprising:

- forming an impurity region 206 (n+ region) in a device region 203/206/207 of a substrate 201/202/Si layer (i.e. a semiconductor-on-insulator substrate), the impurity region 206 defining a pn junction 215;
- forming a buried amorphous region in the device region, i.e. forming a buried amorphous silicon layer (i.e. a first buried amorphous region), wherein the 203/206 resides, on an amorphous insulating layer 202 (i.e. a second buried amorphous region) as the semiconductor-on-insulator substrate (col. 2, lines 15-27; col. 35, lines 6-16);
- forming at least two dislocation regions D in the device region 203/206/207, one of the at least two dislocation regions D being formed by annealing the semiconductor-on-insulating substrate to recrystallize the buried amorphous region (col. 34, line 58 through col. 35, line 16), the dislocation regions D traversing the pn junctions 215 (col. 4, lines 30-33); and
- forming a gate electrode 205 on the device region 203/206/207.

In re claims 2-3 and 8-9, Yoshimi et al also teach that the forming of the impurity region comprises forming a source/drain extension region 206 and another impurity region 207 overlapping the source/drain extension region 206, wherein the source/drain extension region 206 and the another impurity region 207 are formed by ion implantation, i.e. by implanting Ge ions (col. 3, line 34; col. 4, lines 15-18).

In re claim 12, Yoshimi et al also teach that the forming of the at least two dislocation regions D comprises forming at least two buried amorphous region (i.e. the aforementioned first and second buried amorphous regions) in the device region 203/206/207 and heating the semiconductor-on-insulator substrate to recrystallize the at least two buried amorphous regions (col. 34, line 58 through col. 35, line 16).

In re claims 6 and 13, Yoshimi et al further teach that the forming of the at least two buried amorphous regions comprises implanting a neutral species ions (i.e. germanium ions) into the device region 203/206/207, i.e. implanting Ge into the device region 203/206/207 to form SiGe region 207 (Fig.7 and col. 4, lines 15-22).

In re claim 10, Yoshimi et al. also teach that a first of the at least two dislocation regions D (i.e. the dislocation at the left side of a region 203) traverses a portion of the junction 215 proximate the source/drain extension region 206 and a second of the at least two dislocations D (i.e. the dislocation at the right side of a region 203) traverses a portion of the junction 215 proximate the another impurity region 206 because Yoshimi et al. clearly teaches that crystal defect region D, which is the dislocation, would traverse the pn junction interface 215 over the drain region 206 and the channel region 203 (col. 4, lines 30-33 and Fig.7).

In re claims 14 and 17, Yoshimi et al., in Fig. 7 and related text, teach the claimed method of processing, comprising:

- forming a first impurity region 206 (i.e. a region 206 at the left side of channel 203) and a second impurity region 206 (i.e. another region 206 at the right side of channel 203) in a device region 203/206/207 of a semiconductor-on-insulator substrate 201/202, the first impurity region 206 defining a first junction 215 (i.e. the 215 on the left side of the channel 203) and the second impurity region 206 defining a second junction 215 (i.e. the 215 on the right side of the channel 203);
- forming a first buried amorphous region 202 and a second buried amorphous region 206 in the device region 203/206/207 (col. 2, lines 15-27; col. 35, lines 6-16); and
- forming a first dislocation region D (i.e. the dislocation D at the left side of a channel region 203) and a second dislocation region D (i.e. the dislocation D at the right side of the channel region 203) in the device region 203/206/207 by annealing the semiconductor-on-insulating substrate to recrystallize the first and second buried amorphous region 202 and 206 (col. 34, line 58 through col. 35, line 16), the first dislocation region D traversing the first junction 215 (i.e. the one on the left side of the channel 203); and the second dislocation region D traversing the second junction 215 (i.e. the one on the right side of the channel 203); and
- forming a gate electrode 205 on the device region 203/206/207 (Fig. 7).

In re claims 15-16, Yoshimi et al also teach that the forming of the first impurity region comprises forming a first source/drain extension region 206 (i.e. the 206 at left side of 203) and a first overlapping impurity region 207 overlapping the source/drain extension region 206, and the forming of the second impurity region comprises forming a second source/drain extension region 206 (i.e. the 206 at right side of 203) and a second overlapping impurity region 207 overlapping the second source/drain extension region 206, wherein the first and second source/drain extension region 206 and the first and second overlapping impurity region 207 are formed by ion implantation, i.e. germanium ions are implanted, as stated above.

In re claim 20, Yoshimi et al further teach that the forming of the first and second buried amorphous regions comprises implanting neutral species ions (i.e. germanium ions) into the device region, as stated above.

In re claims 21-27, with the aforementioned teachings, Yoshimi et al. disclose a circuit device, wherein the circuit device comprises a gate electrode 205 (claim 25), comprising:

- a semiconductor-on-insulator substrate 201/202/Si layer having a device region 203/206/207;
- an impurity region 206/207 in the device region 203/206/207, the impurity region 206/207 defining a junction 215, wherein the impurity region 206/207 comprises an extension region 206 and an overlapping region 207 (claim 22);
and
- a first dislocation region D and a second dislocation D in the device region 203/206/207, the first and second dislocation regions D being in non-parallel

spatial relationship and traversing the junction 215 proximate the extension region 206 (claim 23) and first dislocation region D traverses the junction proximate the overlapping region 207 (claim 24), wherein the circuit device comprises a plurality of dislocation regions D traversing the junction 215 (claim 26) and the device region 203/206/207 comprises silicon (claim 27).

In re claims 28-33, with the aforementioned teachings, Yoshimi et al. further disclose a circuit device, wherein the circuit device comprises a gate electrode 205 (claim 32), comprising:

- a semiconductor-on-insulator substrate 201/202/Si layer having a device region 203/206/207;
- a first impurity region 206/207 (i.e. the region 206/207 at the left side of 203) in the device region 203/206/207, the first impurity region 206/207 having a first extension region 206 and defining a first junction 215 (i.e. the first 215 at the left side of 203);
- a second impurity region 206/207 (i.e. the region 206/207 at the right side of 203) in the device region 203/206/207, the second impurity region 206/207 having a second extension region 206 and defining a second junction 215 (i.e. the second 215 at the right side of 203), the second junction 215 being separated from the first junction 215 to define a channel 203;
- a first dislocation region D in the device region 203/206/207 (i.e. the D at the left side of 203), the first dislocation region D traversing the first junction 215 proximate the first extension region 206 and the first overlapping region 207 (claim 29); and

- a second dislocation region D in the device region 203/206/207 (i.e. the D at the right side of 203), the second dislocation region D traversing the second junction 215 proximate the second extension region 206 (claim 30) and the second overlapping region 207, the circuit device comprises a first plurality of dislocation regions D (i.e. the plurality of dislocation regions D at left side of 203) traversing the first junction 215 and a second plurality of dislocation regions D (i.e. the plurality of dislocation regions D at right side of 203) traversing the second junctions 215 (claim 31); and the device region 203/206/207 comprises silicon (claim 33).

Response to Arguments

5. Applicant's arguments filed 10/9/03 have been fully considered but they are not persuasive.

In re amended claim 1, applicant argued that Yoshimi et al. do not disclose "the formation of a dislocation region by first forming a buried amorphous region and thereafter annealing to recrystallize the buried amorphous region." (last paragraph, page 8).

Contrary to the argument, Yoshimi et al. do teach the aforementioned limitation. In particular, Yoshimi et al. teach that the semiconductor-on-insulator substrate (i.e. SOI) can be formed of an *amorphous* Si layer on an insulating film, wherein the insulating layer is formed of *amorphous* as well (col. 2, lines 15-19). Yoshimi et al., in Fig. 7 and related text in col.34, line 58 through col. 35, line 31, disclose that the formation of crystal defects D (i.e. dislocation region) is performed by first forming a buried amorphous region, which is *equivalent to the buried amorphous Si layer where regions*

203, 206 and 207 are located, and thereafter annealing to recrystallize the buried amorphous region. The conditions for forming the dislocation depend on the *annealing* temperature and Ge dose (col. 35, lines 1-2); and the formation of the dislocations is by means of twinning mechanism in the course of *recrystallization* process of the *amorphous silicon* (col. 35, lines 6-16). By doing so, junction leakage current can be reduced (col. 35, lines 30-31).

In re claim 2, applicant argued that “Yoshimi et al. does not disclose the formation of a dislocation region in conjunction with a dual graded source/drain region, that is, one that includes a source/drain extension region and an overlapping impurity region. The source/drain region 206 disclosed in FIG. 7 of Yoshimi et al. is a single graded source/drain region.” (second paragraph, page 9).

Contrary to the argument, Yoshimi et al. do teach the formation of a dislocation region D in conjunction with a source/drain extension region 206 and an overlapping impurity region 207, as illustrated in Fig.7. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., “single graded” or “dual graded”) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

In re claims 3 and 4, Yoshimi et al. teach the claimed limitations, as stated above.

In re claims 6 and 7, the word “buried” also appears in Yoshimi et al. (col. 28, line 63); and the formation of one of two dislocation regions D is conducted by annealing the substrate to recrystallize the buried amorphous region, as stated above. A *buried*

oxide region 202 in Fig. 7 is equivalent to the *aforementioned second buried amorphous region*, whereas an amorphous silicon layer (i.e. where regions 203, 206 and 207 are located) is *equivalent to the aforementioned first buried amorphous region*. Because Yoshimi et al. clearly indicate that the semiconductor-on-insulator substrate (i.e. includes regions 201, 202, 206 and 207 in Fig. 7) can be formed of an *amorphous* Si layer (i.e. equivalent to the first amorphous region) on an insulating film (i.e. equivalent to the second amorphous region), wherein the insulating layer is formed of *amorphous* as well (col. 2, lines 15-19). The *buried amorphous region* is formed by implanting neutral species ions (i.e. Ge ions) into the device region, i.e. forming a Ge-doped region (SiGe region 207) in the buried amorphous region.

In re claims 8, 9, 10 and 11, Yoshimi et al. also teach the claimed limitations, as stated above.

In re claims 12 and 13, Yoshimi et al. teach the formation of two buried amorphous regions, i.e. the aforementioned first and second buried amorphous regions, a dislocation region D traversing a junction 215 (col. 4, lines 30-33); and implanting neutral species ions (i.e. Ge ions) into the device region, as stated above.

In re claims 15, 16 and 17, Yoshimi et al. further teach the claimed limitations, as stated above.

In re amended claim 20, Yoshimi et al. further teach forming the aforementioned first and second buried amorphous regions comprising implanting neutral species ions (i.e. Ge ions) into the device region, as stated above.

In re claims 21, Yoshimi et al. further teach the first dislocation region D (i.e. the defects D on the left side of the channel 203), the second dislocation region D (i.e. the

defects D on the right side of the channel 203) and the first and second dislocation regions D being in non-parallel spatial relationship and traversing the junction 215, as stated above and illustrated in Fig. 7.

In re claims 22-28, Yoshimi et al. further teach the claimed limitations, including the first impurity region (i.e. the region 206/207 at the left side of 203) having a first extension region 206 and an overlapping region 207; and the second impurity region (i.e. the region 206/207 at the right side of 203) having a second extension region 206 and another overlapping region 207; and teach a device including source/drain extension regions 206 and dislocation regions D traversing the junctions 215 of those source/drain regions, as stated above.

In re claim 29-33, Yoshimi et al. also teach the claimed limitations, as stated above.

For the above reasons, the rejection is deemed proper.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsien-Ming Lee whose telephone number is 703-305-7341. The examiner can normally be reached on M-F (9:00 ~ 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703-306-2794. The fax phone number for the organization where this application or proceeding is assigned is 703-308-7382.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Hsien-Ming Lee
Examiner
Art Unit 2823

Dec. 19, 2003

A handwritten signature in cursive script, reading "Hsien Ming Lee", with a long horizontal flourish extending to the right.